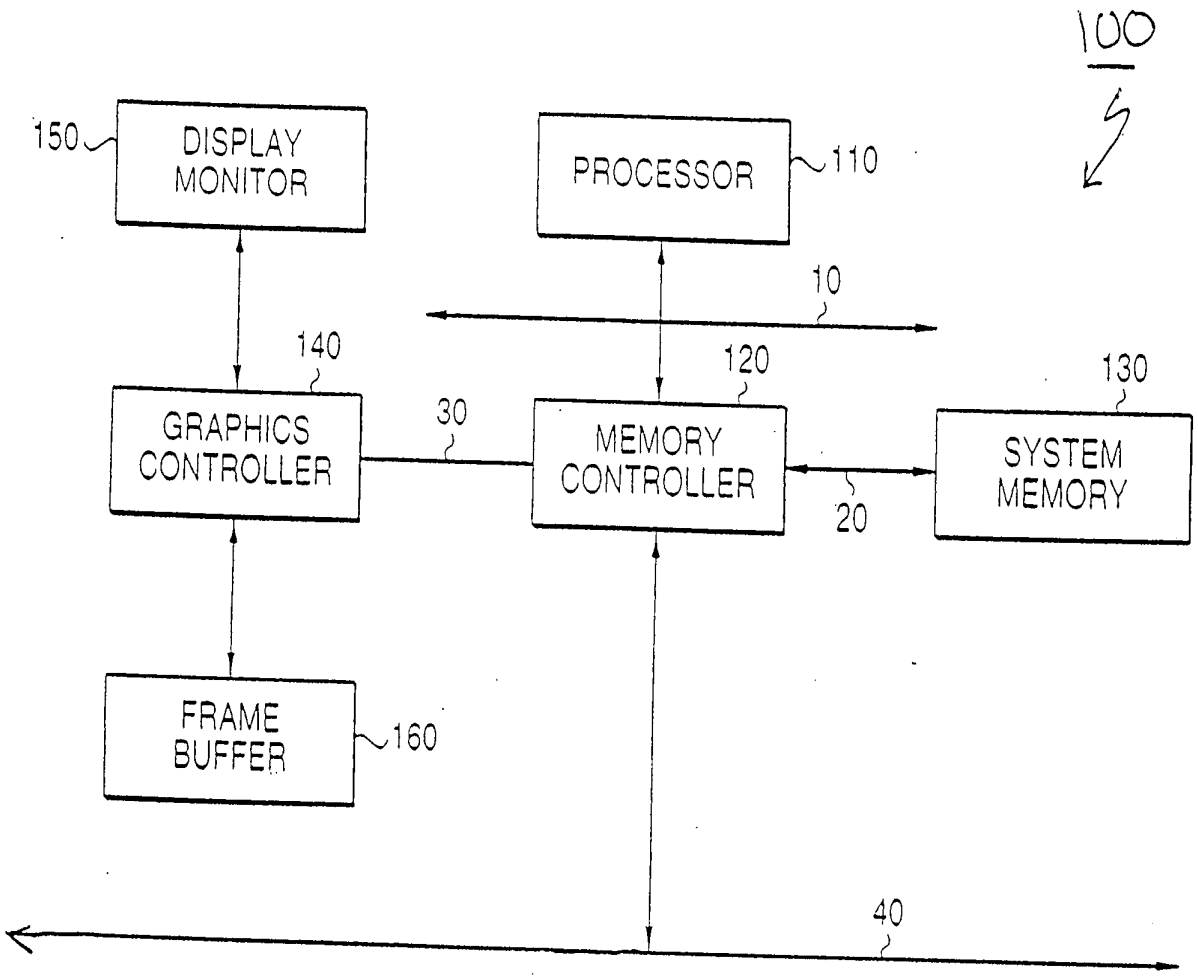


FIG. 1

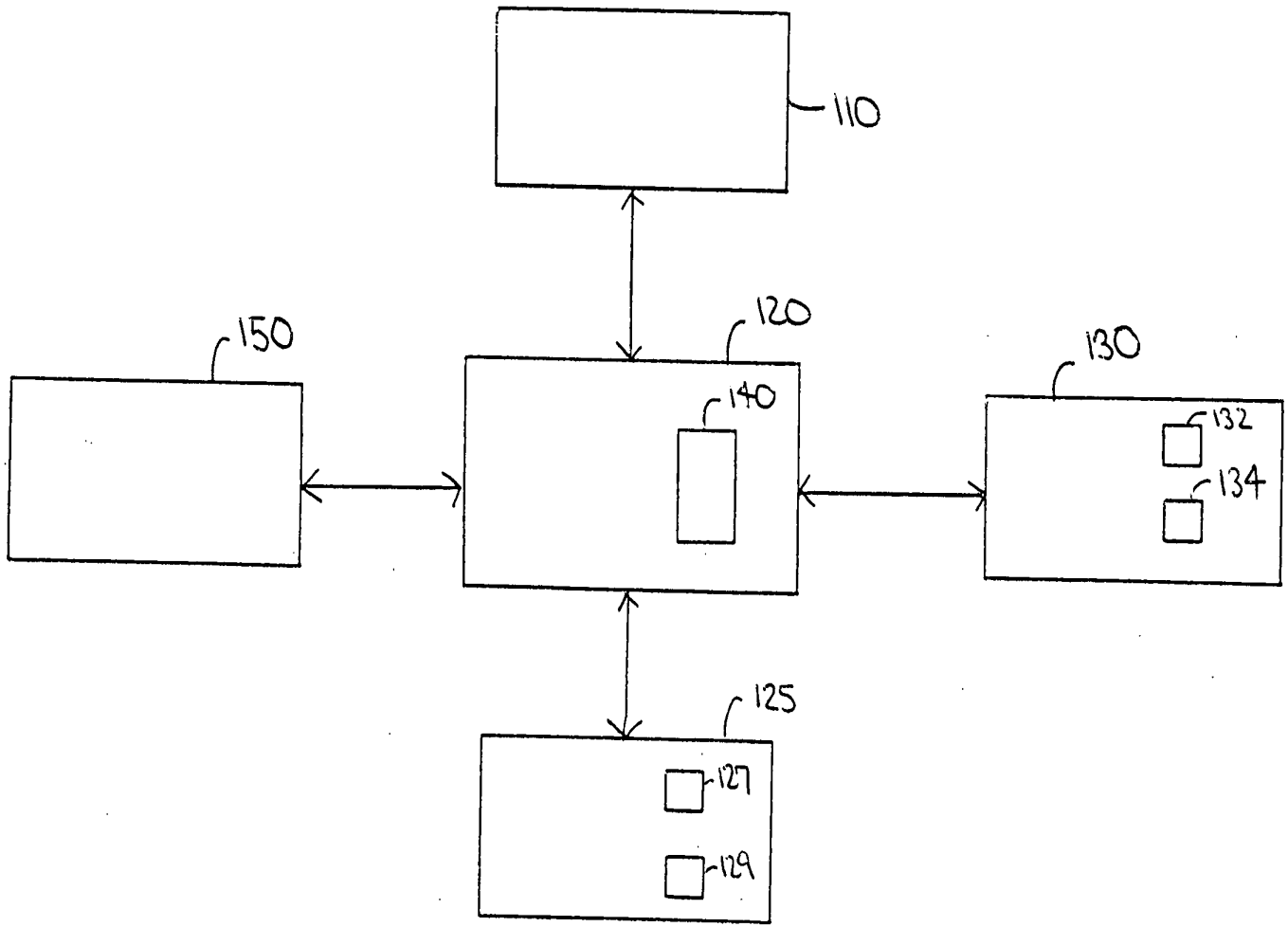


FIG. 2

FIG.3

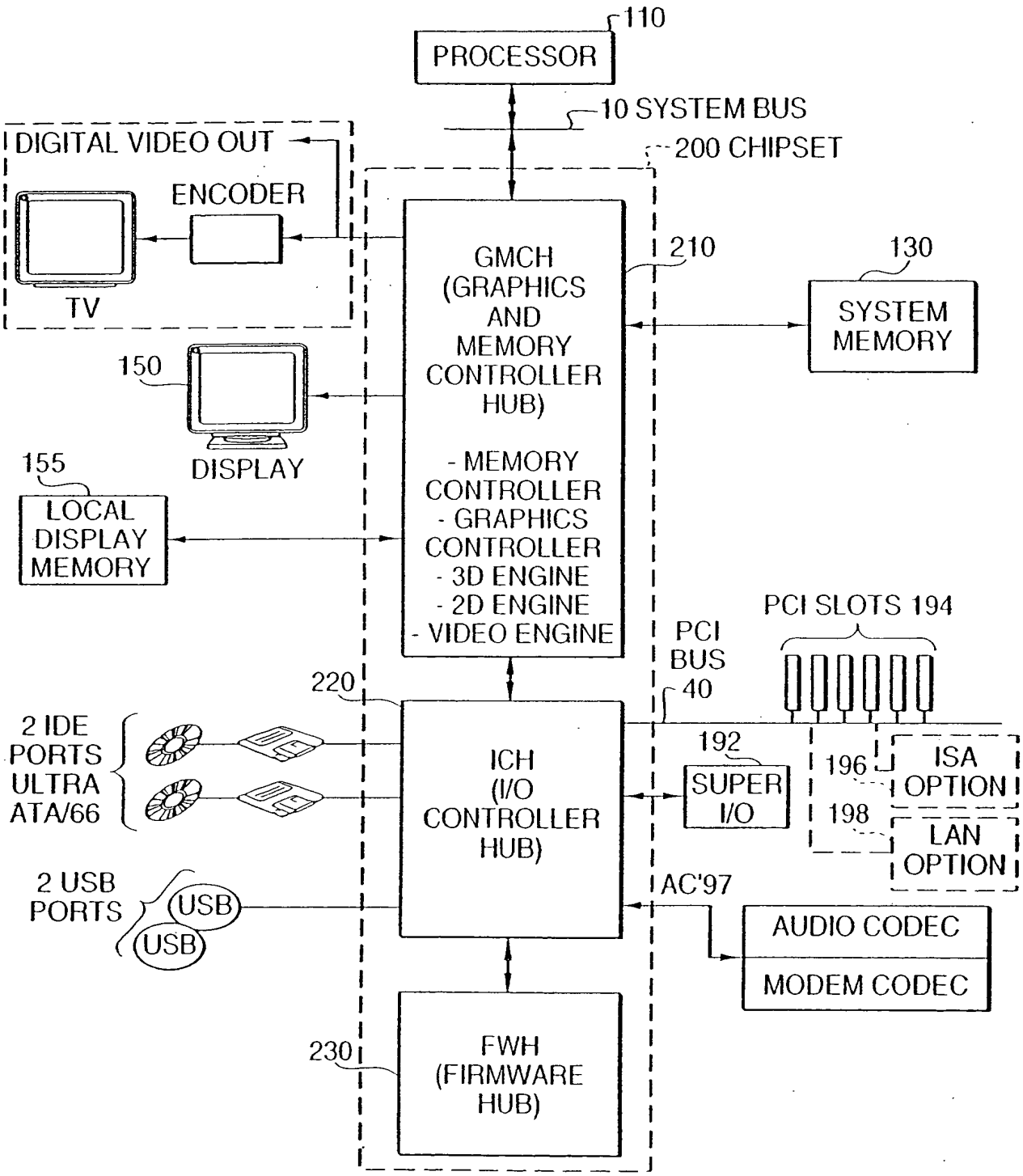
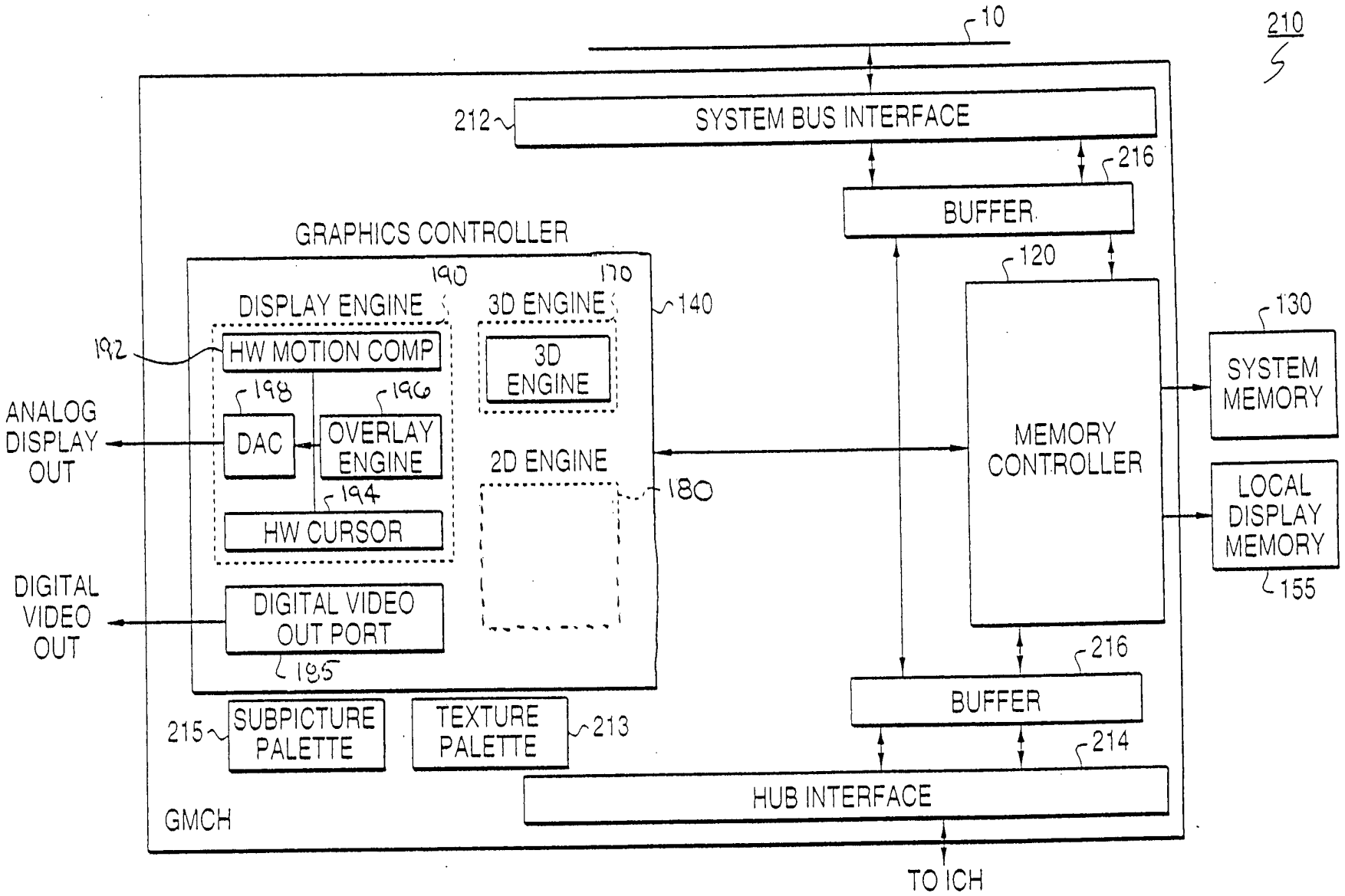

110
PROCESSOR
10 SYSTEM BUS
200 CHIPSET
DIGITAL VIDEO OUT
ENCODER
TV
GMCH (GRAPHICS AND MEMORY CONTROLLER HUB)
- MEMORY CONTROLLER
- GRAPHICS CONTROLLER
- 3D ENGINE
- 2D ENGINE
- VIDEO ENGINE
210
130
SYSTEM MEMORY
150
DISPLAY
155
LOCAL DISPLAY MEMORY
PCI SLOTS 194
PCI BUS 40
220
2 IDE PORTS ULTRA ATA/66
ICH (I/O CONTROLLER HUB)
192
SUPER I/O
196
198
ISA OPTION
LAN OPTION
2 USB PORTS
USB
USB
AC'97
AUDIO CODEC
MODEM CODEC
230
FWH (FIRMWARE HUB)

FIG. 4


10
210
212
SYSTEM BUS INTERFACE
216
BUFFER
GRAPHICS CONTROLLER
190
170
DISPLAY ENGINE
3D ENGINE
140
120
130
192
HW MOTION COMP
3D ENGINE
SYSTEM MEMORY
198
196
ANALOG DISPLAY OUT
DAC
OVERLAY ENGINE
2D ENGINE
MEMORY CONTROLLER
180
194
HW CURSOR
LOCAL DISPLAY MEMORY
155
DIGITAL VIDEO OUT
DIGITAL VIDEO OUT PORT
195
216
BUFFER
215
SUBPICTURE PALETTE
TEXTURE PALETTE
213
214
HUB INTERFACE
GMCH
TO ICH

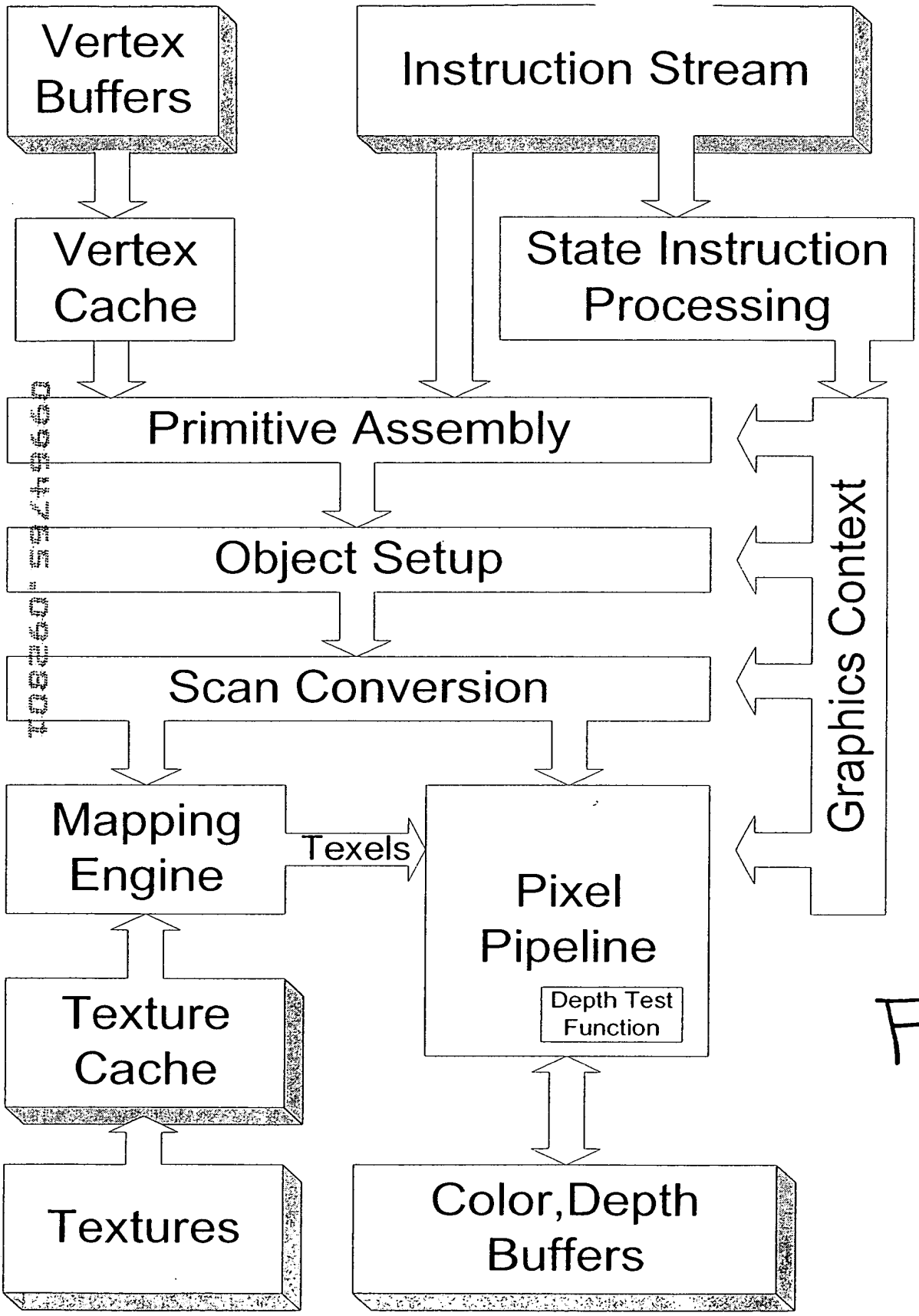

Vertex Buffers
Instruction Stream
Vertex Cache
State Instruction Processing
Primitive Assembly
Object Setup
Scan Conversion
Graphics Context
Mapping Engine
Texels
Pixel Pipeline
Depth Test Function
Texture Cache
Textures
Color,Depth Buffers

FIG.5

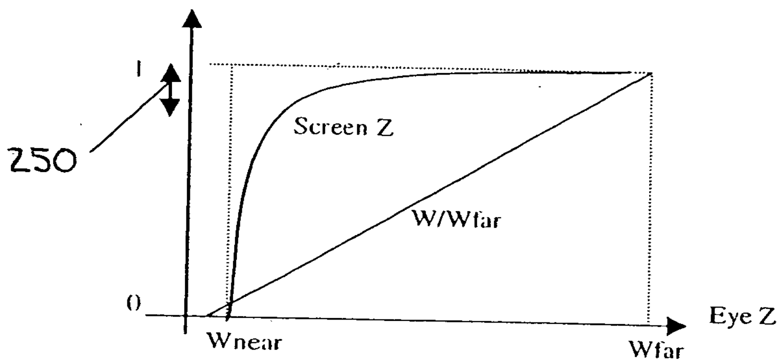


FIG. 6

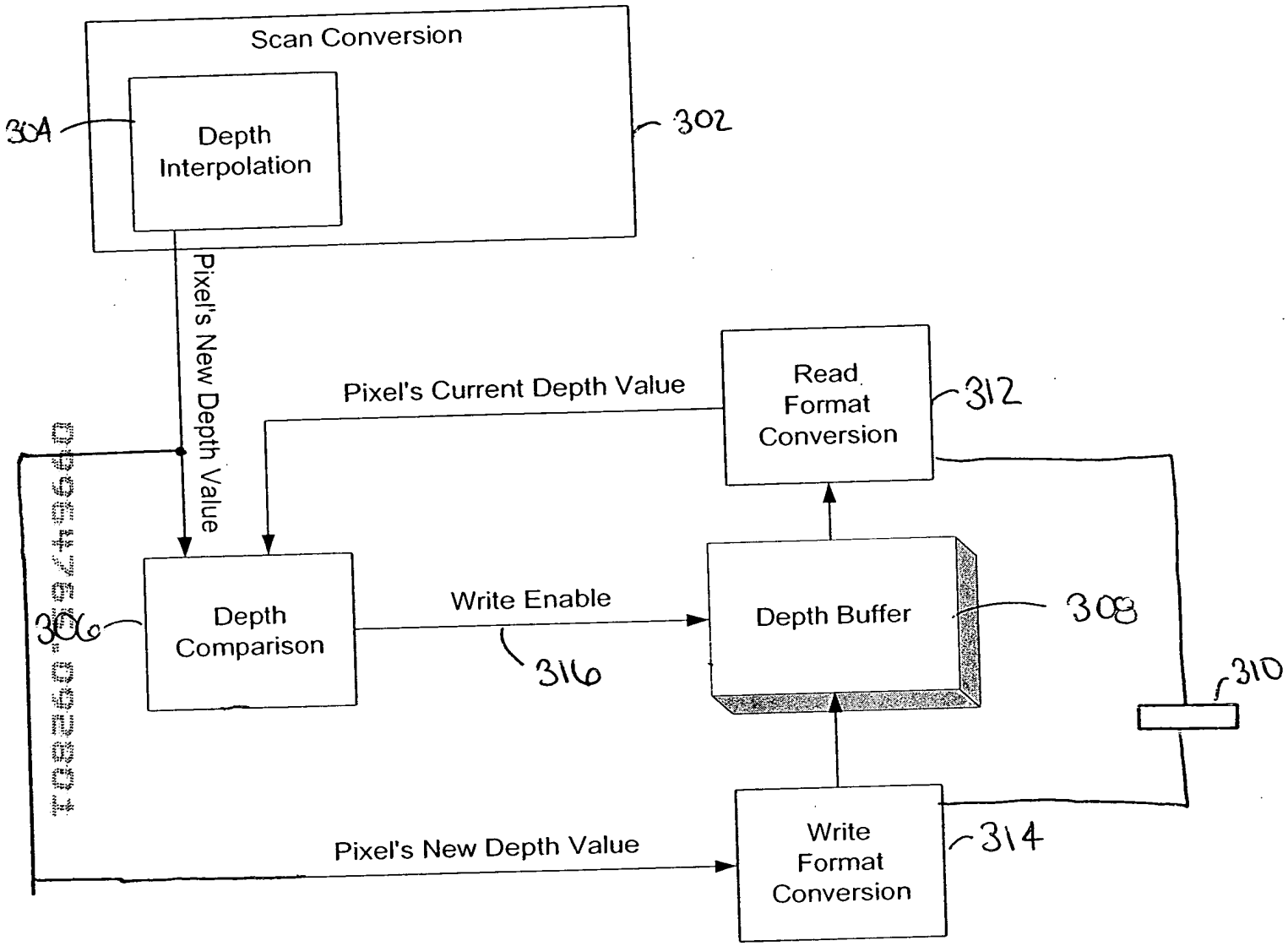
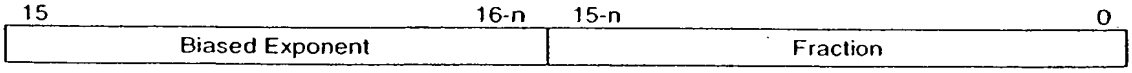

Scan Conversion
304
Depth Interpolation
302
Pixel's New Depth Value
Pixel's Current Depth Value
Read Format Conversion
312
Depth Comparison
306
Write Enable
316
Depth Buffer
308
310
Write Format Conversion
314
Pixel's New Depth Value

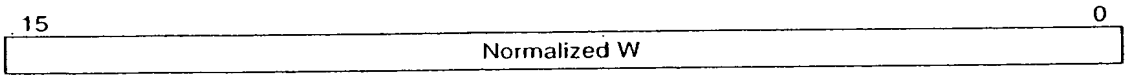
FIG. 7

FIG. 8A



Bit	Description
15:16-n	**Biased Exponent:** Format: n-bit unsigned biased exponent, where n = *WExponentSelect*. The exponent is biased by 2^n.
15-n:0	**Fraction:** Format: (16-n)-bit fractional portion of the floating point significand.

FIG. 8B

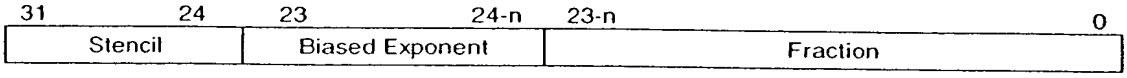


Bit	Description
15:0	**Normalized W (W/Wfar):** Format: U0.16 Range = [0,1)

FIG. 8C

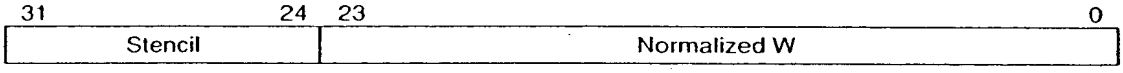
Biased Exponent (n bits)	Significand		Represented Value (W/WFar)
	Integer	Fraction	
exp = 0..2^n-1	1	frac	1.frac * 2^(exp-2^n)

FIG. 9A



Bit	Description
31:24	**Stencil:** Format: U8 Range = [0,255]
23:24-n	**Biased Exponent:** Format: n-bit unsigned biased exponent, where n = *WExponentSelect*. The exponent is biased by 2^n.
23-n:0	**Fraction:** Format: (16-n)-bit fractional portion of the floating point significand.

FIG. 9B



Bit	Description
31:24	**Stencil:** Format: U8 Range = [0,255]
23:0	**Normalized W (W/Wfar):** Format: U0.24 Range = [0,1)